SNO pFEC System Test Results

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1 Introduction

The SNO electronics chain [1], shown in Figure 1, provides deadtimeless sub-nanosecond time and charge measurement for photomultiplier (PMT) pulses in the range of 1 - 1000 photo electrons. The electronics chain must handle background radioactivity rates in excess of 1 kHz and potential astrophysical burst rates in excess of 1 MHz. The basic functionality and performance of the system are set by the three full custom integrated circuits that provide all of the high speed signal processing functions. These circuits are:

IC Name	Function	Process
SNOD	pulse discriminator and timer	AT&T CBICU-II
SNOINT	dual precision charge integrator	AT&T CBICU-II
QUSN6	analog memory & TAC with event sparsification	NT CMOS4s

Initial tests of these circuits were carried out in dedicated bench set ups at Penn and Queen's as well as by using the Penn HP82000 integrated circuit test facility. These tests were very encouraging and indicated that individually each circuit performed largely as designed and was likely to be capable of meeting or exceeding the requirements of the experiment. These tests are described in [2] and [3] and documented in various internal notes.

In this note we wish to show the result of a series of measurements made using the prototype eight channel front end card (pFEC). The pFEC was specifically designed to allow us to measure the interactions of the three chips with each other and with the commercial components that will make up the rest of the dataflow in the production electronics. This data flow is indicated schematically in Figure 2. On the pFEC the blocks surrounding the QUSN6 chip (indicated in the figure as the 16 Cell Analog/Digital Memory) were implemented using standard commercial parts of the class that we plan to use in the production electronics. The control of the readout sequence is provided by a round robin polling engine implemented in a Xilinx FPGA. The ADC function is provided by four Maxim MAX120 2μsec 12 bit ADCs. The 4 MB Dram is a standard 1 $\times$ 36 80 ns SIMM controlled by a Phillips dual port memory controller. The VME interface is a simple A32, D32 slave. We have examined the integrity of the digital signal processing - Trigger I.D. consistency, simultaneous writes and reads into the memory block, correct functioning of the VME interface, ability to work in an asynchronous fashion, high (up to 4MHz event rate) and low rate stability, etc. - and have found no problems. We will concentrate on the more difficult analog measurements in the rest of this note.

The pFEC board(s) are mounted in a standard J1/J2 VME backplane controlled by a Macintosh Quadra 950 using a Bit3 interface card. The Macintosh ran the prototype DAQ code provided by the University of Washington / LANL group. The code was modified and extended at Penn to match the pFEC hardware details. Using this setup it is possible to acquire events at a DC rate in excess of 50kHz (but for a small number of operating channels) or a burst rate of up to 4 MHz.

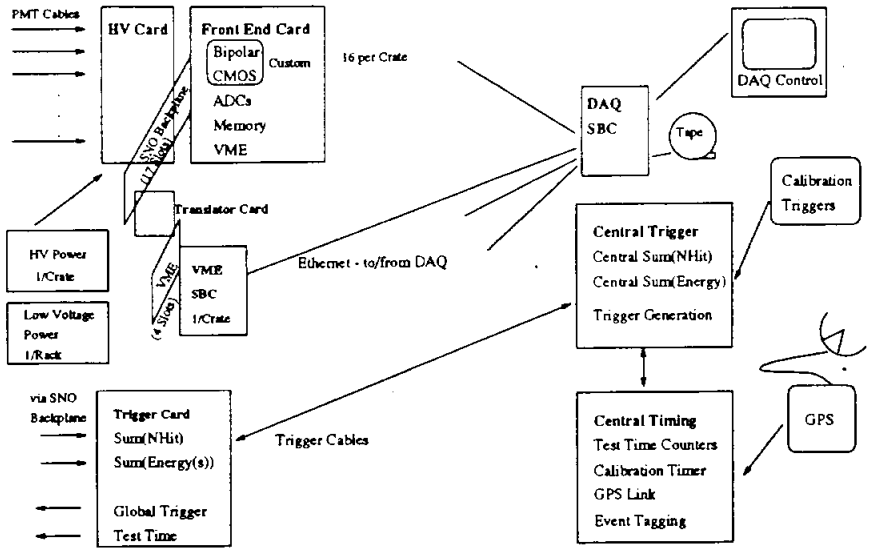

Figure 1: Block diagram of the SNO electronics system. The crate level electronics on the left side of the figure are repeated 20 times, and connect to the central system on the right of the figure.

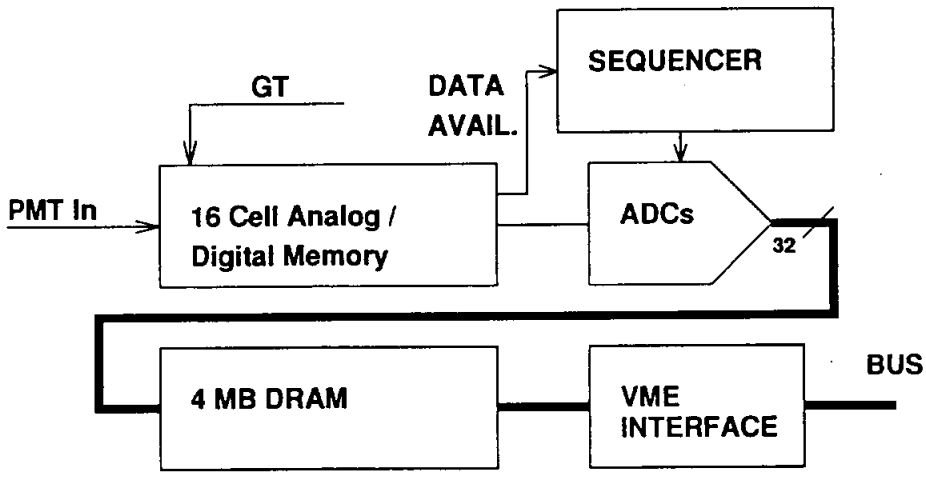

Figure 2: On board data flow from the PMT inputs to the VME interface.

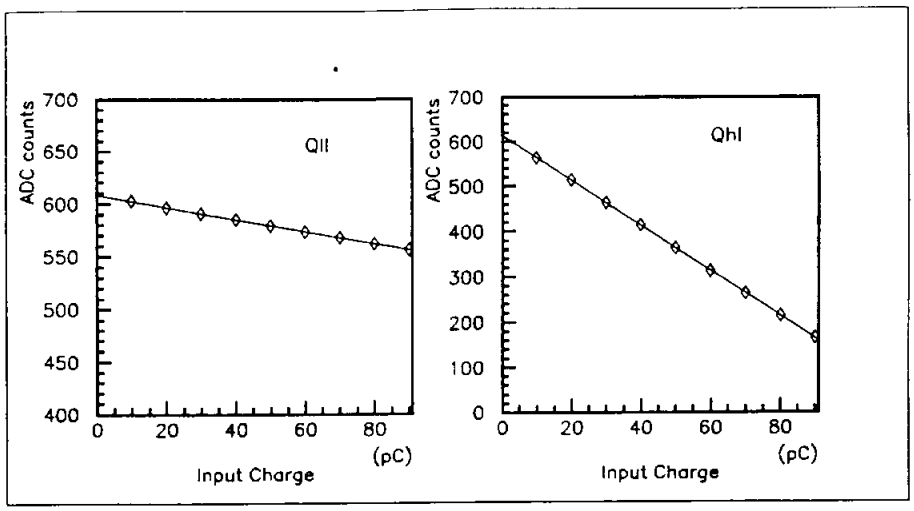

Figure 3: Pulser measurements of charge linearity for Q Low Gain Long Integrate, left and Q High Gain Long Integrate, right. One photoelectron produces about one pC. Additional tests were run over both smaller and larger charge ranges with similar results.

2 Pulser Tests

Once all the basic board blocks were shown to be operational (memory, ADCs, etc.) initial tests of the front end chips were made using precision pulsers. Pulse injection was either as an analog pulse put in at the pFEC PMT input connector in a fashion similar to the planned HVCard interface or via the built in pedestal self test facility which accepts a differential ECL timing pulse off of the crate backplane. The measurements below were made using the entire SNO pFEC data path. The entire system, from the SNOD chips through the Macintosh, was run at rates exceeding those needed for the experiment, data was reformatted using a program linked against SNOLIB 2.07 which allowed us to analyze the data using the preproduction SNO analysis package SNOMAN 2.07.

It should however be noted that all of the pulser measurements in this section were made using only a fraction of the ADC range and that the data in the next section on PMT tests are taken with an operational amplifier gain block before the ADC which gives a factor of 6 improvement in precision for the charge measurements and a factor of 4 for the time measurements.

2.1 Charge Linearity

As can be seen in Figure 3, the charge measurement response is very linear. The difference in slope between the left and right halves of the figure reflects the board level signal attenuator that sets the ratio of the High and Low gain channels. This ratio is yet to be optimized, but very large signal tests have indicated that the linearity is preserved up to at least the 1,000 pe level. The straight line fits shown in Figure 3 show a maximum deviation from a straight line of 1.3 counts [1] over the range of 10 to 110 pC and a maximum deviation of only 0.29 counts in the critical region 1.2 to 11 pC [2]. The fit is characterized by a quite respectable χ^2 of 10 for 7 degrees of freedom.

[1] For Q High Short, the numbers for the other two samples are better - Q Low Long has a maximum deviation of only 0.62 counts over the 10 -110 pC range.

[2] This fit is from a separate run, not shown here, covering the 0-20 pC range. There are about 4 counts per pC in these measurements which were taken prior to the addition of a gain (×6) block before the ADC.

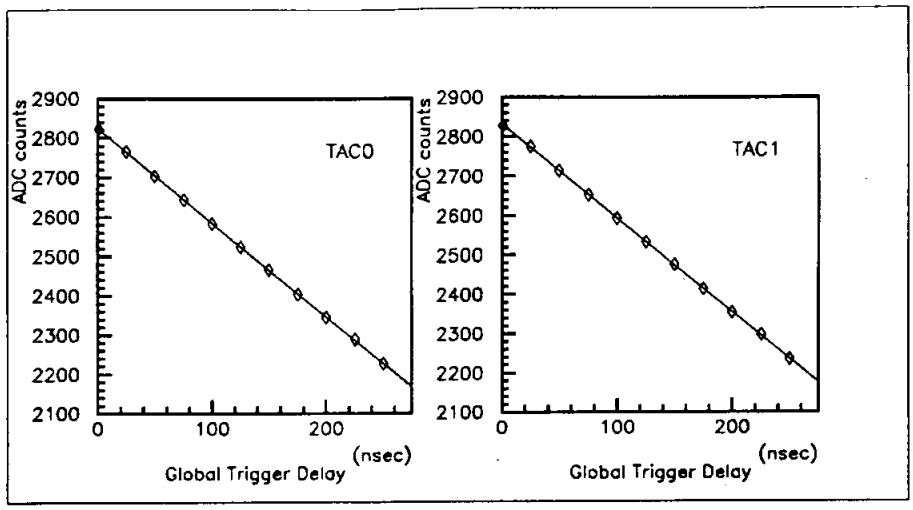

Figure 4: Pulser measurements of the TAC linearity using the primary current source. The 250 nsec range is roughly the design range for the TAC. TAC0 and TAC1 are two *ping pong* devices to allow deadtimeless operation.

2.2 Time Linearity

Since we wish to keep very high availability for each channel, we have provided paired Time to Amplitude Converts (TACs) which operate in a ping pong fashion. Schematically the TACs are current sources which are switched from a dummy load to a measuring capacitor during the time measurement process. At the end of the time measurement the current source is switched back to the dummy load and the voltage on the capacitor reflects the elapsed time. In addition to the current source and the capacitor there are reset switches to pull the capacitor back up to the quiescent level and output buffer amplifiers to drive the stored voltage out of the cell to the output during a read cycle. As can be seen in Figure 4, both TACs are linear. The straight line fit to the TAC0 data has a slope of -2.4 counts/ns $\pm 0.1\%$. TAC1 is almost identical in slope. The fit has a χ^2 of 22 for 9 degrees of freedom and the integral non-linearity is about 0.5nsec. The worst case differential non-linearity is about 1 nsec. Precision measurements using the full 12 bit ADC range will be necessary to accurately characterize the TACs.[3]

2.3 Cell Offsets

Since the QUSN6 chip has separate storage capacitors and buffer amplifiers for each of the sixteen possible samples, it is important to measure the cell to cell matching. We have looked at charge and time measurements [4] for both slope changes and pedestal offsets. The slopes for all cases match very well and there is, as would be expected for a CMOS process, a small mismatch in the pedestal value cell to cell. Figure 5 shows the pedestal variation for the sixteen Q High Gain Long cells in test chip

[3] Until very recently the current mirror inputs on QUSN6 (isetm0 or isetm1) were not capacitively bypassed at the chip and on-board coupling to the discriminator signal led to a quadratic term in the time measurement. For a long time this was thought to have been a problem with either the TAC circuit design or the actual silicon processing. Proper on-board bypass procedures have eliminated this behavior and the even more puzzling differences in response between TAC0 and TAC1.

[4] There are three different samples of charge and one time measurement for each PMT hit - Q High Gain Long, Q High Gain Short, Q Low Gain Long, and the TAC value. Here Long and Short are the integration sampling times set by the SAMPLE pulse out of the SNOD chip, typically 30 and 200 ns, and Low and High are the inverse of the relative attenuation applied prior to the two separate integrator channels.

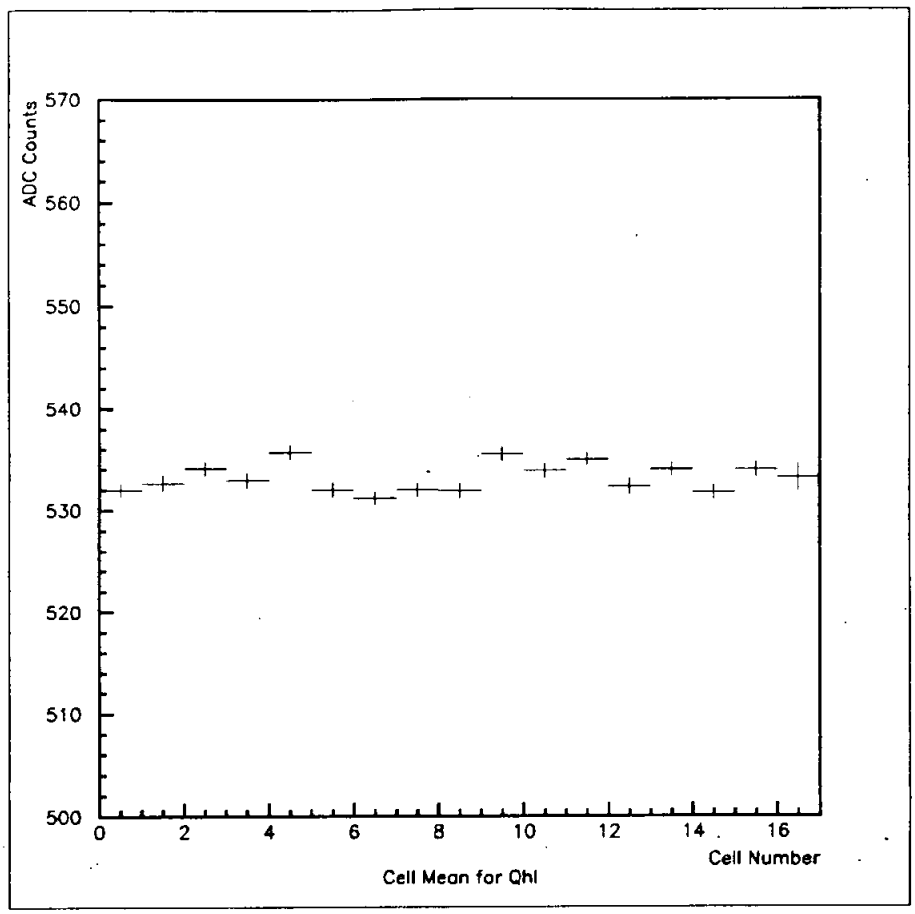

Figure 5: Pulser measurements of the cell to cell offsets inside the QUSN6 chip. One ADC count corresponds to 2.5mV at the QUSN6 output.

serial number 6, which is typical. The seventeenth point plotted is the mean of the 16 pedestals (533.17 with an RMS error of 1.38 ADC counts). The RMS on any individual cell is about 0.7 counts or less than 2 mV. The actual RMS may be somewhat less as these measurements were made using only a portion of the ADC range, effectively 10 bits, and full accuracy measurements are typically even tighter. Note that the scale here is about 45 ADC counts per pC or about 35 ADC counts per photo electron (pe), thus while the pedestals vary measurably, the actual effect on the precision of our measurement would only be a modest fraction of a pe even before correction/calibration.

2.4 Trigger Outputs

One of the very useful, but last minute, additions to the electronics functionality was the inclusion of programmable delay and width Trigger output signals on the QUSN6 chip. The idea is to have programmable control over both a normal (nominal 100ns wide) and test (nominal 20ns wide) output which is used to make an analog sum of NHit. The circuitry consists of a series of programmable width generators (selectable delays used to reset a flip flop) initiated by the same discriminator pulse from SNOD which starts the QUSN6 TAC. The output of this circuit is a switchable current source to allow for simple board level analog sums. The programmable width and delay (20ns only)

functions have been tested and shown to work well. However, because of the last minute nature of this inclusion, an error in the specification led to the omission of an internal pull up on the output current drive. Thus when the Trigger output current source is connected to the outside world through the output transmission gate, the current source has been in saturation attempting to pull against an infinite load and takes some time to return to equilibrium after the front edge of the pulse. This results in a significant ($\times 2$) overshoot for the first 4-5ns of the output followed by a few ns of undershoot and then stable operation. While the overshoot is not fatal, it does make the shape of the trigger turn on curve very mushy and should be removed if possible. Fortunately, a trivial fix will provide the missing pull up transistor. This transistor can be laid out by hand within the area already occupied by the Trigger output circuitry and connected in a straightforward fashion to the correct polarity line driving the transmission gate so that the new transistor is on when the gate is off and *vice versa*. Because this change is important, but involves a very minor layout change and should be very low risk, we recommend that this change be made in the production version of QUSN6. The new layout would, of course, be extracted and the complete chip would be run through a few hundred ns of SPICE simulation to verify the change.

3 PMT Tests

While pulser tests are useful for understanding many types of problems, they can not fully provide the level of confidence necessary to base an experiment on a given circuit. Only use of the real sensor element, realistically stimulated, can demonstrate that the electronics will perform as required in the experiment. With this in mind, we borrowed several real [5] SNO R1408 PMTs from Queen's and made a small scale dark room containing the R1408s, a few 2" monitoring PMTs, a radioactive source and scintillator and a high rate sonoluminescence source.

3.1 Setup

Two of the R1408's are configured at this time as trigger detectors and feed into conventional electronics while the third tube is connected to the pFEC setup via a realistic 105 ft. of RG59. This is the tube that was used in the tests described below. All three tubes are set up to view either the scintillator or sonoball and various apertures may be applied to the face of the test tube to explore various levels of illumination. The trigger signal generated by the coincidence of the trigger tubes may be delayed and used to generate a Global Trigger (GT) for the pFEC or the GT may be generated by a pulser.

3.2 Pedestals

Prior to looking at real distributions, it is necessary to measure the pedestal (effectively the zero reference for the measurement) position and width. Figure 6 shows that the pedestal measurement obtained using the SNOD pedestal enable input (PEN) and a properly timed GT signal. The pedestal position is stable over the time that we have looked at the system and the width (FWHM = 2 counts where one pe is about 30 counts) is gratifyingly narrow. This test was done with the PMT and cable attached and HV applied but with an extra opaque cover on the PMT to ensure that no external photons were recorded [6]. The actual pedestal measurement is made in response to a pulser input on the SNOD *pedestal* input.

We have also looked at the time pedestal and, as can be seen in Figure 7, these pedestals too are quite narrow, about 3-4 bins FWHM where there are about 11 bins per ns. There is a small offset between TAC0 and TAC1 as would be expected.

[5] Except that the base was not waterproofed.

[6] In some runs a few hits at about 1 pe were recorded, presumably from photocathode thermal emission.

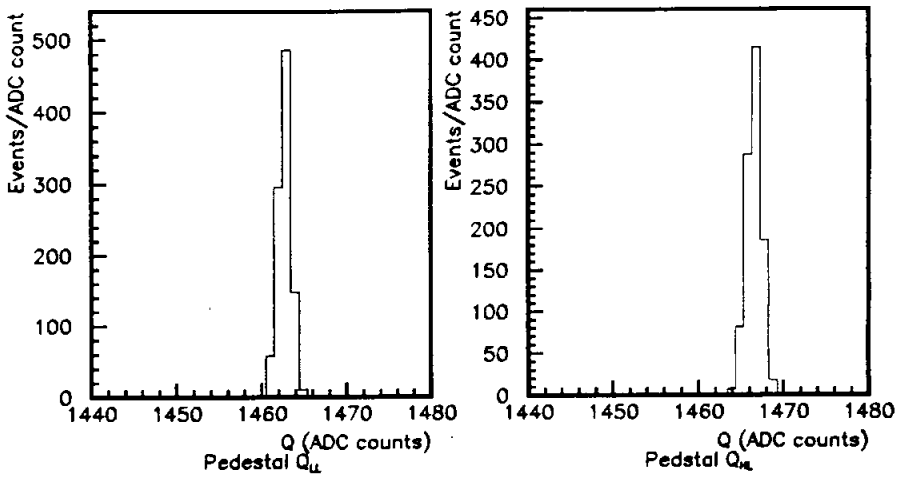

Figure 6: Pedestal distribution for Q Low Long on the left and Q High Long on the right.

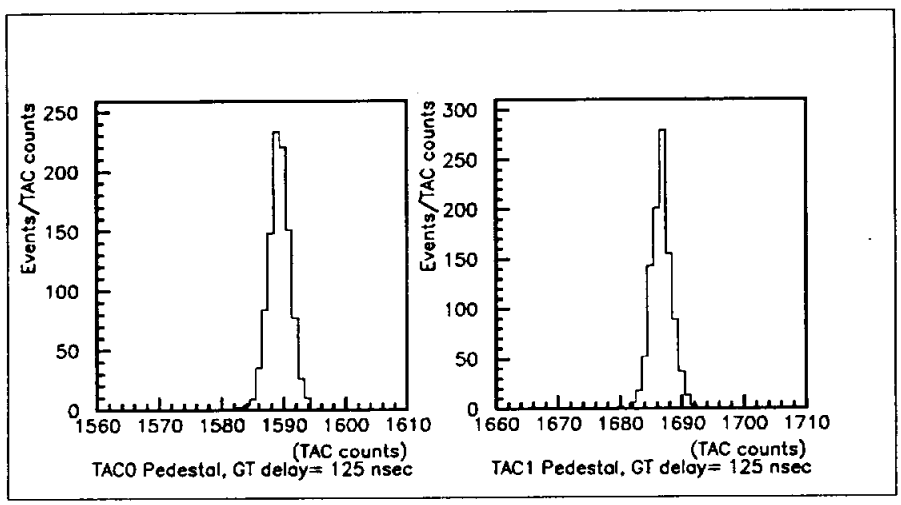

Figure 7: Pedestal distributions for TAC0 on the left and TAC1 on the right. One ns is about 12 counts.

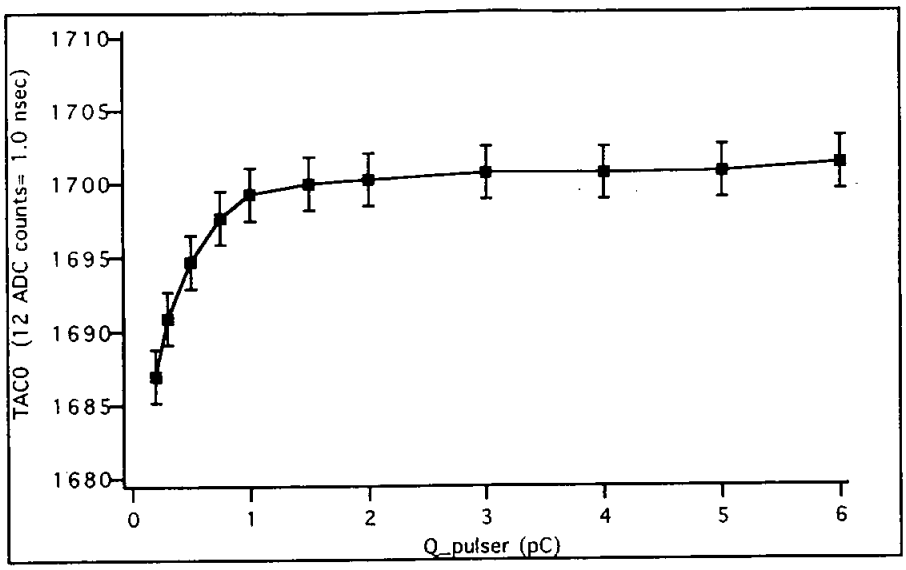

Figure 8: Change in time measurement vs. input charge over 0 to 6 pC. The *discriminator walk* is partially due to the finite (1-2 ns) pulser rise time and partially due to the inherent discriminator response time. Further measurements will be necessary to entirely unfold these effects.

An additional figure of merit is the discriminator walk. Near threshold any comparator will require somewhat longer to respond than with a relatively large overdrive. In Figure 8 it can be seen that there is slightly more than 1 ns of change in response time going from 0.2 to 6 pC (about $\frac{1}{6}$ to 5 pe). Some of this time walk is due to the finite rise time of the pulser used for this test (about 1^+ ns). With a real PMT pulse, of course, the observed walk will be dominated by the 4-5 ns rise time of the PMT signal - in which case the data will require a correction of the measured time for the walk induced by different pulse heights near threshold.

3.3 Single pe Tests

SNO is a large dynamic range experiment, requiring precision at the single photoelectron level and accuracy at large signal levels. It is essential that the electronics be optimally sensitive to single pe signals. Using either the scintillator or sonoball sources it is possible to see the single pe signal with high [7] efficiency and accuracy. Figure 9 shows the distribution obtained with a relatively low threshold. The beginnings of the exponential rise of noise hits is visible on the left and a clear valley is evident between the noise and the single pe peak. For comparison with ordinary units, one can note that the nominal average gain of the PMTs is 10^7 so that a single photo-electron will produce 1.6×10^{-12} C of charge. This pico-Coulomb will then produce two equal currents - one branch into the PMT base back termination and the other into the 75Ω RG-59 transmission line. Thus a nominal pe gives us 0.8 pC into the 75Ω termination at the pFEC. For a PMT pulse with a baseline width of about 16 ns, this implies a peak current of about $100\mu A$ or 7.5mV on the termination. We are setting thresholds in the range[8] of $\frac{1}{10}$ to $\frac{1}{20}$ of a pe or on the order of 800 to 400 μV. With no HV on the PMTs, the system is quiet at the lowest thresholds.

Because the SNOD discriminator function works as a leading edge discriminator, it is necessary to adjust the measured time of a hit by the pulse amplitude to correct for the finite PMT pulse rise

[7] But as yet not fully quantified.

[8] Again this needs careful calibration and is hostage to a variety of different interpretations of means, averages, etc., so care should be used in interpreting these numbers.

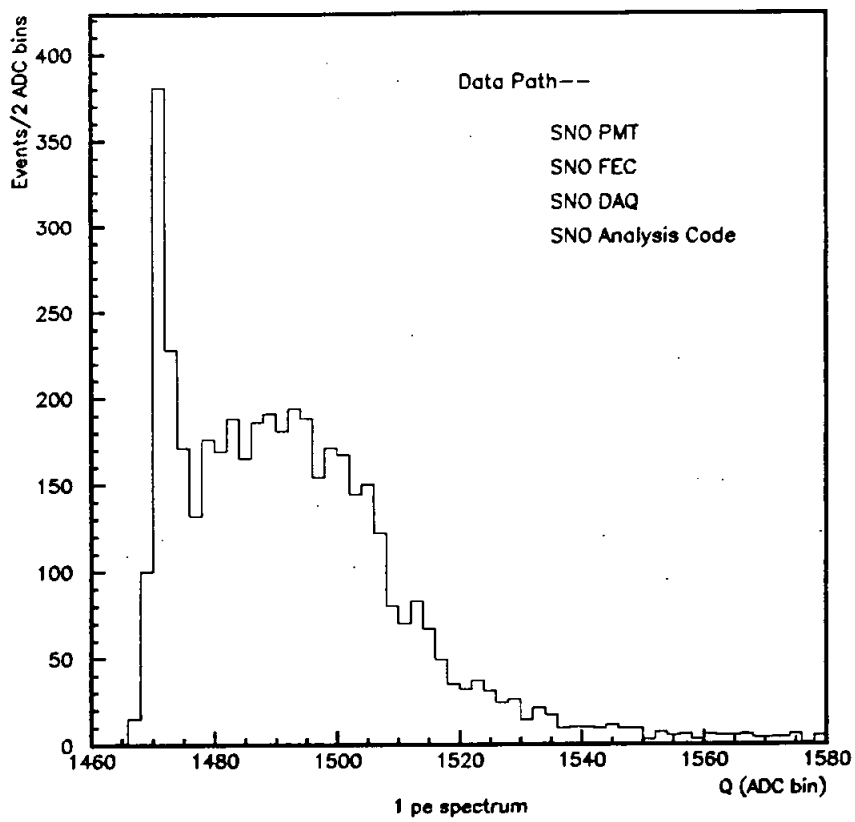

Figure 9: Single photo electron peak from a SNO 1408 PMT, SNO base, and 105' RG59 cable. The light source was a scintillator with an attached radioactive source. The optical efficiency was set to less than 10% to ensure a low contamination from multiple pe events.

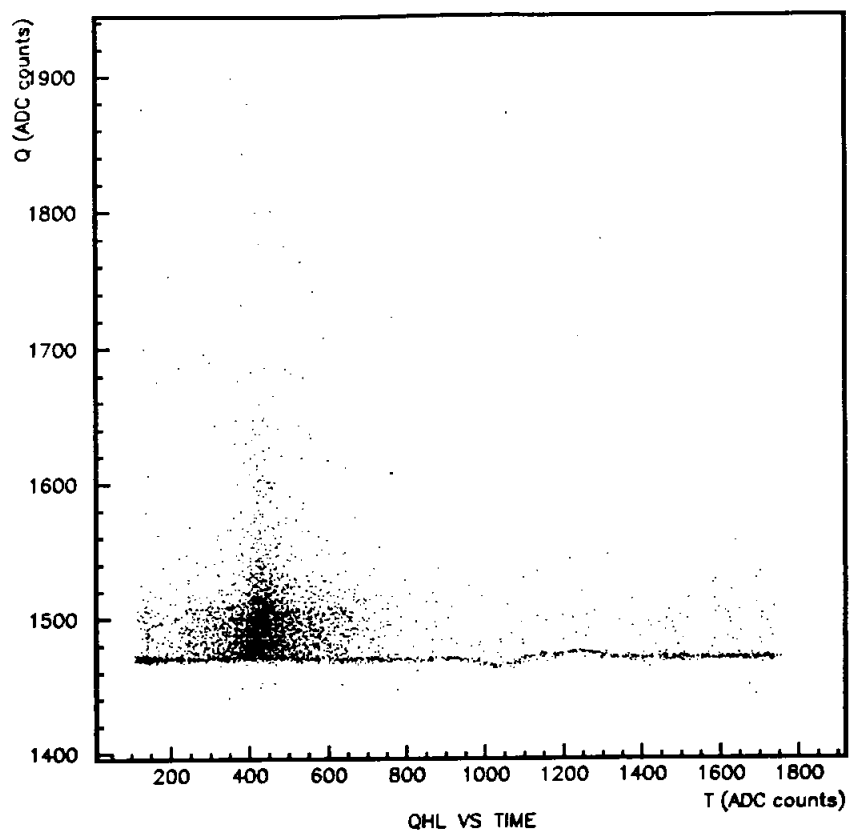

Figure 10: Single photo electron events plotted as Charge vs. Time for Q High Gain Long. The single pe distribution is clearly visible as a clustered smudge and the beginnings of the noise distribution as the horizontal line near Q=1470.

time and the discriminator's time response variation with delivered input energy. In the present test set up, the trigger has an inherent jitter from the trigger PMTs plus somewhat antiquated low sensitivity trigger electronics. Thus the Q vs. T (charge vs. TAC time) scatter plot in Figure 10 shows little correlation between the measurements although we would expect to see a few nano second effect over the 0.1 to 2 pe range (the present crude calibration is that there are about 7 counts per ns on the time axis and about 30 counts per pe on the charge axis). One effect that is, however, quite striking is the small ripple in the effective charge baseline at around 1100 counts in time. We believe that this ripple is caused by pickup or feedthrough from the trigger signal or GT into either the PMT cable (which runs near the rack of trigger electronics) or actually on the board or even internally in the QUSN6 chip. We expect to pursue and identify (and hopefully remove) this effect over the next week or two. The important point to note here is the extreme sensitivity of the system and the ability that we have here to look for subtle second order effects. The ripple indicated here would correspond to an impulse of about 2 mV amplitude at the input to QUSN6 and less than 1 mV at the input to the integrator. But even if the effect is an irremediable feature of the QUSN6 layout, it corresponds to only a small fraction of one pe during a small part of the sensitive time.

To begin to understand the ripple effect shown in Figure 10 we also looked at the Q High Gain Short integrator which should not show any such effect because the integral is complete after about 30ns. As Figure 11 demonstrates the ripple is indeed gone, but there is a new feature at T of about

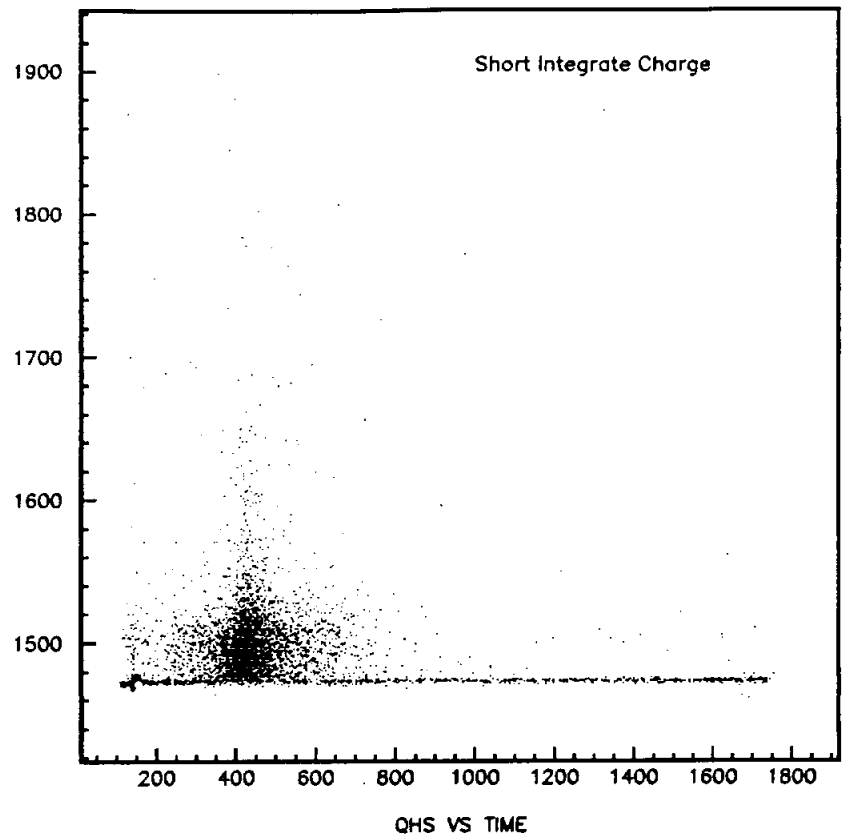

Figure 11: Single photo electron events for Q High Gain Short Integrate plotted as Charge vs. Time. The single pe distribution is clearly visible as a clustered smudge and the beginnings of the noise distribution as the horizontal line near Q=1470. Note that the baseline wave evident in Fig. 9 at T about 1000-1200 is no longer evident because the integrator has closed off at an earlier time, but now some structure exists at T of about 180.

180 - again probably a low level crosstalk or pickup effect, but one that would be impossible to see without the full system.

Another obvious test at this point is to cut the single pe data set on time of arrival in order to improve the signal to noise. Figure 12 shows the same data but only looking at T bins from 375 to 475 counts (about ± 8 ns). The clear Poisson shape indicates that there is nothing fishy about the signal and will allow us to make a reasonable estimate of efficiency for any given threshold setting.

4 Multi pe Tests

In order to understand whether or not the low gain, high charge part of the integrator-storage system (SNOINT/QUSN6) is working properly, we tested the system using the sonoluminescent source being developed by D. McDonald and W. Frati. This sonoball was placed a few feet from the PMT under test and ran at a steady 23kHz rate. Figure 13 shows the hit distribution. A small remnant pedestal may indicate some misfirings in the sonoball. There are about 3 counts per pe on this range, so about 500 pe into the PMT. The width of this distribution is dominated by variations in the pulse to pulse intensity ($\sim 10\%\sigma$) of the sonoball.

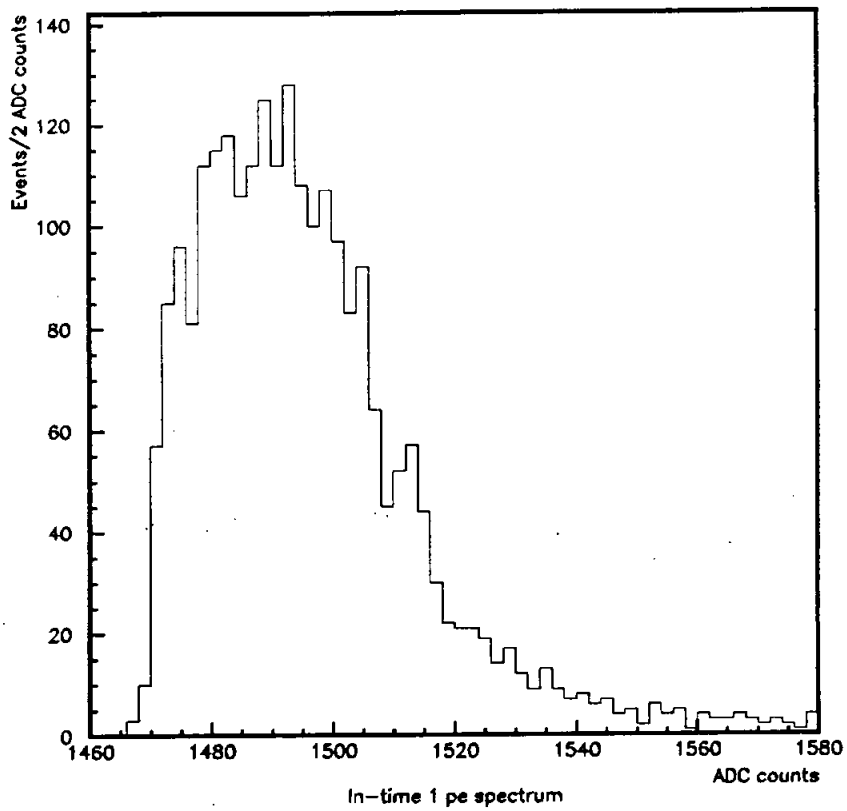

Figure 12: Single photo electron peak as in the previous Figure, but with the distribution cut by excluding events (noise) more than ± 8ns away from the nominal trigger time.

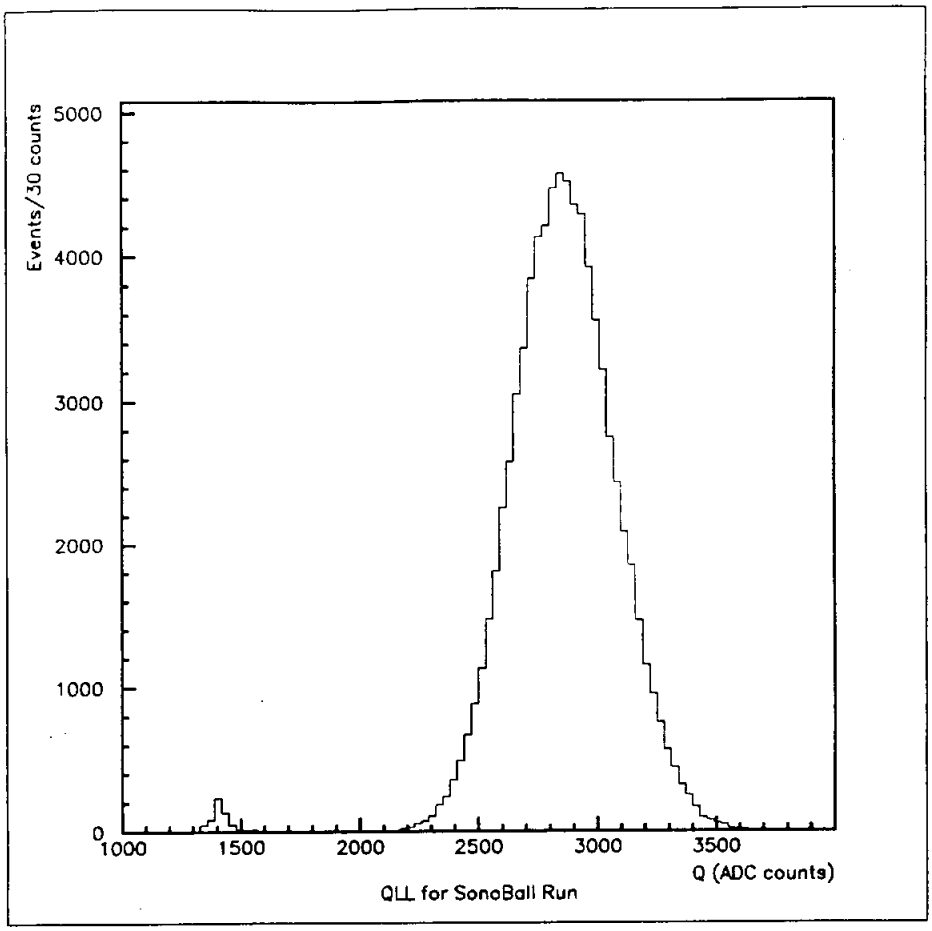

Figure 13: Multi photo electron peak from a SNO 1408 PMT, SNO base, and 105' RG59 cable. The light source was the sonoball sonoluminescent light source. This is the Q Low Gain Long Integrate output. The pedestal is clearly visible at about 1400 counts - probably because of occasional cosmic ray induced triggers. The calibration for this output is about 3 counts per pe so the sonoball is giving about 500 pe into the 4" optical aperture used here. At full aperture the system saturates as would be expected.

The Low Gain calibration of about 3 counts per pe is set by the input attenuator at the SNOINT inputs. With the present arrangement the system saturates at about 800 pe. We intend to optimize the attenuation ratio to better match the Hamamatsu R1408 tube. For instance a Low Gain scale of about 1 ADC count per pe (and a slight adjustment of the pedestal position) would yield a full scale of $> 3,000$ pe or a *channel* dynamic range of order 16 bits[9]. The detector dynamic range is, of course, limited at the low end to a single pe, but at the high end we could, almost inconceivably, deal with 9,456 PMTs with 3,000 pe each or from 1 to nearly 30×10^6 pe.

5 Conclusion

The SNO chip set works as intended and can be read out using prototypes of the entire data chain. Realistic PMT inputs behave well, the precision and accuracy of the measurements matches or exceeds our requirements, and we believe that we are ready to begin production of the devices.

[9] With 30 to 40 counts per pe at the low end, extending the range to 3,000 pe produces a full range of 90,000 to 120,000 counts

Additional tests are clearly indicated to understand the variety of second order effects (e.g. the apparent GT correlated pickup on the charge channels) and some details of signal termination on the board, but there are no *show stoppers.*

5.1 Chip Modifications for Production

Based on our bench tests and these board level tests, we plan to make the following, *but only the following*, changes and modifications to the custom integrated circuits prior to production:

1. SNOD
   (a) Reroute bus lines to accommodate design rule changes to improve yield.
   (b) Change V_{CCA} distribution to a fully symmetric form to reduce possible low level cross talk.
   (c) Change MET1 routing near resistors to accommodate design rule changes and improve yield.
2. SNOINT
   (a) Add damping resistors to the Integrator Monitor outpus to control possible feedback oscillations.
3. QUSN6
   (a) Add current source pull up transistor to Trig_100 and Trig_20 outputs to avoid large overshoots on the front edge of the trigger outputs.

5.2 Future Work

The next clear milestone is to acquire multi PMT data from the University of Washington test pool and this will go forward as soon as the rest of the prototype QUSN6 chips have been packaged and mounted on the boards. A future note will cover results from that test set up.

In parallel, we plan to begin layout on the final 32 channel FEC boards and associated support items (backplane, translator card, trigger card, timing and trigger logic, etc.) for the final production system.

References

[1] T. Ekenberg, F.M. Newcomer, R. Van Berg, A. Biman, R.L. Stevenson; *The Sudbury Neutrino Observatory Electronics Chain* , submitted to IEEE Transactions on Nuclear Science, Proceedings of the Nuclear Science Symposium, Nov. 1994.

[2] F.M. Newcomer and R. Van Berg; *A Wide Dynamic Range Integrator-Discriminator-Timer Chip Set for PMT Applications* , submitted to IEEE Transactions on Nuclear Science, Proceedings of the Nuclear Science Symposium, Nov. 1994.

[3] T. Ekenberg, F.M. Newcomer, R. Van Berg, A. Biman, R.L. Stevenson; *An Analog Memory, Time to Amplitude Converter, and Trigger Logic Chip for PMT Applications* , submitted to IEEE Transactions on Nuclear Science, Proceedings of the Nuclear Science Symposium, Nov. 1994.